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Amendment

REMARKS

The claims have been amended without adding new matter in order to correct minor informalities and to address other issues raised by the Examiner. Specifically, claims 1, 45, and 52-54 have been amended, and claim 51 has been canceled in addition to claims 6-9, and 28-31 which were previously cancelled. Forty seven (47) claims remain pending in the application: Claims 1-5, 10-27, 32-50, and 52-56. Reconsideration of the pending claims in view of the amendments above and remarks below is respectfully requested.

By way of this amendment, Applicants have made a diligent effort to place the claims and application in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned at (858) 552-1311 so that such issues may be resolved as expeditiously as possible.

Applicants thank the Examiner for indicating that claims 51 and 52 are allowable subject matter, and the suggested language that would make the claims more likely to be in condition for allowance. Claim 45 has been amended to include the limitations of claim 51. Therefore, Applicants believe that independent claim 45 as amended is now in condition for allowance as well as all of claims 46-50 and 52 which depend from claim 45. Further, Applicants have amended claim 1 to incorporate language indicated by the Examiner that would make claim 1 more likely to be allowable.

Turning to the specific rejections:

1. The Examiner has rejected claims 1-5, 10, 11, 16, 17, 19-27, 32, 33, 38, 39, 41-44, and 53-56 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,005,565 (Legall et al.) in view of U.S. Patent No. 5,923,379 (Patterson).

Applicants have amended claim 1 to recite at least in part,

a buffer logic circuit that receives the digital signals and facilitates communication is coupled with both the circuit that receives wireless television communication signals and the circuit that receives computer network communication signals. . . .

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Similarly, claim 23 recites in part, "buffering and controlling the transfer of commands"
Applicant respectfully submits that the combination of references fails to teach or suggest the apparatus and method of claims 1 and 23.

More specifically with respect to claim 1, for example, neither Legall nor Patterson teach or suggest at least a buffer logic circuit coupled with both a circuit that receives wireless television communication signals and the circuit that receives computer network communication signals to facilitate communication between the two circuits.

Alternatively, the Examiner expressly rejected claim 1 suggesting that a bus shown in Patterson teaches a circuit that receives a digital signal and facilitates communication. However, the "bus" as recited by the Examiner is not a buffer logic circuit, nor a buffer logic circuit that "receives the digital signals and facilitates communication is coupled with both the circuit that receives wireless television communication signals and the circuit that receives computer network communication signals" as recited in claim 1 and described in the subject application. Therefore, amended claim 1 is not taught or made obvious in view of the applied references, and Applicants respectfully request the rejection be withdrawn.

Claims 2-5, and 10-22 depend from amended claim 1. Therefore, these claims are also in condition for allowance for at least the reasons provided above.

The Examiner indicated that independent claim 23 was also rejected over Legall in view of Patterson. However, Applicants respectfully submit that the Legall and Patterson references fail to teach at least buffering and controlling of the transfer of commands as recited in claim 23. The "bus" as cited by the Examiner does not provide buffering or controlling of the transfer of commands and data through a third circuit. More specifically, claim 23 recites at least in part "buffering and controlling the transfer of commands and at least portions of the sensory data and the programming data between the first and second circuits through a third circuit." There is no suggestion or teaching in either Legall or Patterson to provide at least buffering and controlling of the transfer of commands and data through a third circuit as recited in claim 23. The Legall and Patterson references also fail to teach or suggest the buffering and controlling of

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the transfer of data between first and second circuits as claim 23 recites. Applicants respectfully submit that the applied references do not make claim 23 obvious. Therefore, claim 23 is in condition for allowance and Applicants respectfully request the rejection be withdrawn.

Claims 24-27, and 32-44 depend from claim 23. Therefore, these claims are also in condition for allowance for at least the reasons provided above.

2. The Examiner further rejected claims 18 and 40 under 35 U.S.C. § 103(a) over Legall in view of Patterson in further view of U.S. Patent No. 5,081,628 (Maekawa). Applicants respectfully submit, however, that the Maekawa reference also fails to teach or suggest a buffer logic circuit as recited in amended claim 1. Therefore, claims 18 and 40 are not obvious over the applied references and Applicants respectfully request that the rejection be withdrawn.

3. Further, the Examiner rejected claims 12, 13, 34 and 35 under 35 U.S.C. § 103(a) over Legall in view of Patterson in further view of U.S. Patent No. 6,208,384 (Schultheiss). Applicants respectfully submit, however, that Schultheiss also fails to teach or suggest a buffer logic circuit as recited in amended claim 1, or the buffering and controlling of the transfer of commands and data between the two circuits as recited in claim 23. Therefore, claims 12, 13, 34 and 35 are not obvious over the applied references and Applicants respectfully request that the rejection be withdrawn.

4. The Examiner further rejected claims 14, 15, 36 and 37 under 35 U.S.C. § 103(a) over Legall in view of Patterson in further view of U.S. Patent No. 6,212,264 (Maze et al.). Applicants respectfully submit, however, that the Maze et al. reference also fails to teach or suggest a buffer logic circuit as recited in amended claim 1, or the buffering and controlling of the transfer of commands and data as recited in claim 23. Therefore, claims 14, 15, 36 and 37 are not obvious over the applied references and Applicants respectfully request that the rejection be withdrawn.

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5. The Examiner also rejected claims 45-48 and 50 under 35 U.S.C. § 103(a) over Patterson in view of Legall. Independent claim 45 has been amend to incorporate the claim limitation of claim 51, which was indicated by the Examiner as being allowable. Therefore, Applicants respectfully submit that amended claim 45, and claims 46-50 and 52 which depend from claim 45, are now in condition for allowance.

6. Still further, the Examiner rejected claim 49 under 35 U.S.C. § 103(a) over Legall in view of Patterson in further view of Maze et al. As indicated above, however, claim 49 now depends from claim 45 that includes the claim limitation of claim 51 which was indicated as allowable. Therefore, claim 49 is also in condition for allowance.

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CONCLUSION

Applicants submit that the above amendments and remarks place the pending claims in a condition for allowance. Therefore, a Notice of Allowance is respectfully requested.

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Respectfully submitted,



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